What is claimed is:

1. A processor system, comprising:

a first program storage which stores a first program;

a second program storage which stores a second program;

a program counter which outputs execution addresses of said first and second programs;

a first address storage which stores a first address in said first program;

a second address storage which stores a second address in said second program;

a comparator which compares whether or not said program counter coincides with said first address;

an address changing unit which changes said program counter to said second address, when it is determined to have coincided by said comparator; and

a data bus which updates said first address stored in said first address storage and said second address stored in said second address storage.

2. The processor system according to claim 1, further comprising an instruction decoder which provides a result of decoding instructions read out from said first and second program storages to said data bus,

wherein said first address stored in said first address storage and said second address stored in said second address storage are updated based on output of said instruction decoder.

3. The processor system according to claim 2, wherein said first program includes:

a plurality of instructions which store a plurality of first addresses in said first address storage; and

a plurality of instructions which store a plurality of second addresses in said second address storage,

wherein said first address storage stores a plurality of first addresses in sequence, in accordance with said first program at timing different from each other; and

said second address storage stores a plurality of second addresses in sequence, in accordance with said first program at timing different from each other.

4. The processor system according to claim 1, further comprising an interface unit which performs control for storing said first and second addresses supplied from outside, via said data bus, in said first and second program storages.

5. The processor system according to claim 1, wherein said first program storage is an ROM;

said second program storage is a rewritable memory; and

said second program is a program which updates at least portion of said first program.

6. The processor system according to claim 1, wherein said second program is a debug program which performs a debug at an arbitrary location in said first program;

said first address is a head address at a location which performs the debug in said first program; and

said second address is a head address of said debug program.

7. The processor system according to claim 6, further comprising an interface unit which performs control for storing said second program, said first address and said second address supplied from outside via said data bus, in said second program storage, said first address storage and said second address storage, respectively, and performs control for supplying a result of executing

said debug program to outside.

8. A processor, comprising:

a program counter which outputs execution addresses of a first program stored in a first program storage and a second program stored in a second program storage;

a comparator which determines whether or not said program counter coincides with a first address in said first program stored in said first address storage;

an address changing unit which changes said program counter to a second address in said second program stored in said second address storage, when it is determined to have coincided by said comparator; and

a data bus which updates said first address stored in said first address storage and said second address stored in said second address storage.

9. The processor according to claim 8, further comprising an instruction decoder which supplies a result of decoding instructions read out from said first and second program to said data bus,

wherein said first address stored in said first address storage and said second address stored in said second address storage are updated based on the output of said instruction decoder.

10. The processor according to claim 9, wherein said first program includes:

a plurality of instructions which store a plurality of first addresses in said first address storage; and

a plurality of instructions which store a plurality of second addresses in said second address storage,

the processor according to claim 9, further comprising:

a first address storing controller which performs control for storing in sequence a plurality of first

addresses in said first address storage at timing different from each other, in accordance with said first program; and

a second address storing controller which performs control for storing in sequence a plurality of second addresses in said second address storage at timing different from each other, in accordance with said first program.

11. The processor according to claim 8, further comprising an interface unit which performs control for storing said first and second addresses supplied from outside, via said data bus, in said first and second program storages.

12. The processor according to claim 8, wherein said first program storage is an ROM;

said second program storage is a rewritable memory; and

said second program is a program which updates at least portion of said first program.

13. The processor according to claim 8, wherein said second program is a debug program which performs debug at an arbitrary location in said first program;

said first address is a head address at locations which performs debug in said first program; and

said second address is a head address of said debug program.

14. The processor according to claim 13, further comprising an interface unit which perform control for storing said second program, said first address and said second address supplied from outside via said data bus, in said second program storage, said first program storage and said second address storage, respectively,

and performs control for supplying execution result of said debug program to outside.

15. A arithmetic processing method, comprising:

outputting from a program counter execution addresses of a first program stored in a first program storage and a second program stored in a second program storage;

determining whether or not said program counter coincides with a first address in said first program stored in said first address storage; and

changing said program counter into a second address in said second program stored in said second address storage, when it is determined to have coincided.

16. The arithmetic processing method according to claim 15, further comprising

supplying a result of decoding instructions read out from said first and second program storages to said data bus,

wherein said first address stored in said first address storage and said second address stored in said second address storage are updated based on the output of said instruction decoder.

17. The arithmetic processing method according to claim 16, wherein said first program includes:

a plurality of instructions which store a plurality of first addresses in said first address storage; and

a plurality of instructions which store a plurality of second addresses in said second address storage,

and further comprising:

performing control for storing in sequence a plurality of first addresses in said first address storage at timing different from each other, in accordance with said first program; and

performing control for storing in sequence a plurality of second addresses in said second address storage at timing different from each other, in accordance with said first program.

18. The arithmetic processing method according to claim 15, further comprising

performing control for storing said first and second addresses supplied from outside, via said data bus, in said first and second program storages.

19. The arithmetic processing method according to claim 15, wherein said first program storage is an ROM;

said second program storage is a rewritable memory; and

said second program is a program which updates at least portion of said first program.

20. The arithmetic processing method according to claim 15, wherein said second program is a debug program which performs debug at an arbitrary location in said first program;

said first address is a head address at a location which performs debug in said first program; and

said second address is a head address of said debug program.